LM2664 Switched Capacitor Voltage Converter

Check for Samples: LM2664

FEATURES

- Inverts Input Supply Voltage
- 6-Pin SOT-23 Package
- 12Ω Typical Output Impedance
- 91% Typical Conversion Efficiency at 40 mA
- 1µA Typical Shutdown Current

APPLICATIONS

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Suppliers
- Interface Power Suppliers
- Handheld Instruments

DESCRIPTION

The LM2664 CMOS charge-pump voltage converter inverts a positive voltage in the range of +1.8V to +5.5V to the corresponding negative voltage of −1.8V to −5.5V. The LM2664 uses two low cost capacitors to provide up to 40 mA of output current.

The LM2664 operates at 160 kHz oscillator frequency to reduce output resistance and voltage ripple. With an operating current of only 220 µA (operating efficiency greater than 91% with most loads) and 1 µA typical shutdown current, the LM2664 provides ideal performance for battery powered systems. The device is in a SOT-23 package.

Basic Application Circuits

Figure 1. Voltage Inverter

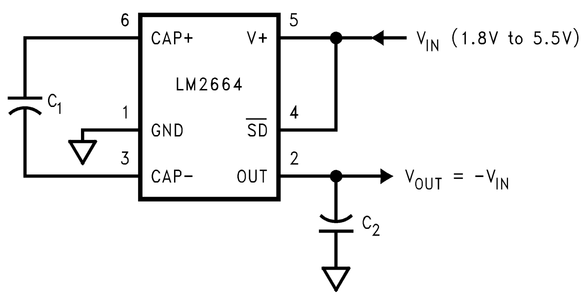
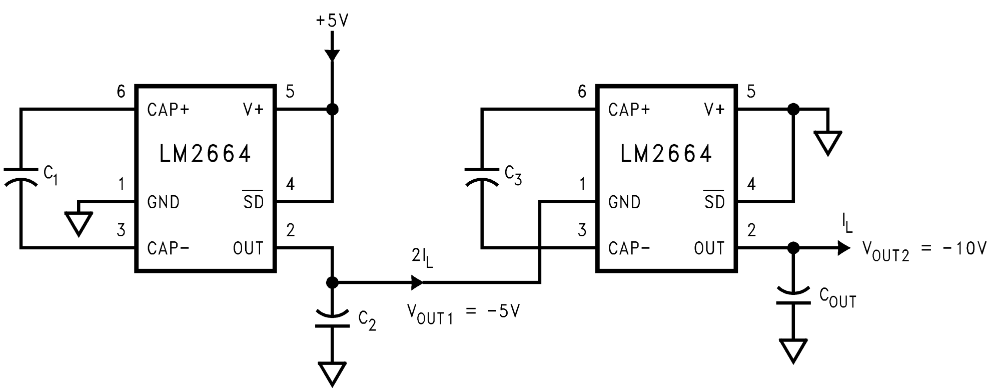


Figure 2. +5V to −10V Converter



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V+ to GND, or GND to OUT)	5.8V
SD	(GND − 0.3V) to (V+ + 0.3V)
V+ and OUT Continuous Output Current	50 mA
Output Short-Circuit Duration to GND[3]	1 sec.
Continuous Power Dissipation (T_A = 25°C)[4]	600 mW
T_{JMax}[4]	150°C
θ_{JA}[4]	210°C/W
Operating Junction Temperature Range	−40° to 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD Rating	2kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/\theta_{JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package.

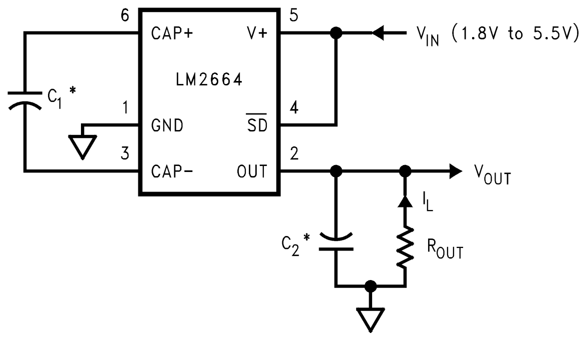
Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V+ = 5V, $C_1 = C_2$ = 3.3 µF.[1]

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V+	Supply Voltage		**1.8**		**5.5**	V
I_Q	Supply Current	No Load		220	**500**	µA
I_{SD}	Shutdown Supply Current			1		µA
V_{SD}	Shutdown Pin Input Voltage	Normal Operation	**2.0** (4)			V
		Shutdown Mode			**0.8** (5)	
I_L	Output Current		**40**			mA
R_{SW}	Sum of the $R_{ds(on)}$ of the four internal MOSFET switches	I_L = 40 mA		4	**8**	Ω
R_{OUT}	Output Resistance[6]	I_L = 40 mA		12	**25**	Ω
f_{OSC}	Oscillator Frequency		(7)**80**	160		kHz
f_{SW}	Switching Frequency	(7)	**40**	80		kHz
P_{EFF}	Power Efficiency	R_L (1.0k) between GND and OUT	**90**	94		%
		I_L = 40 mA to GND		91		
V_{OEFF}	Voltage Conversion Efficiency	No Load	**99**	99.96		%

(1) In the test circuit, capacitors C_1 and C_2 are 3.3 µF, 0.3Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.
(2) Min. and Max. limits are ensured by design, test, or statistical analysis.
(3) Typical numbers are not ensured but represent the most likely norm.
(4) The minimum input high for the shutdown pin equals 40% of V+.
(5) The maximum input low for the shutdown pin equals 20% of V+.
(6) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in the application information for simple negative voltage converter.
(7) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.

TEST CIRCUIT



*C_1 and C_2 are 3.3 µF, SC series OS-CON capacitors.

Figure 3. LM2664 Test Circuit

Typical Performance Characteristics

(Circuit of Figure 3 V+ = 5V unless otherwise specified)

Supply Current vs Supply Voltage

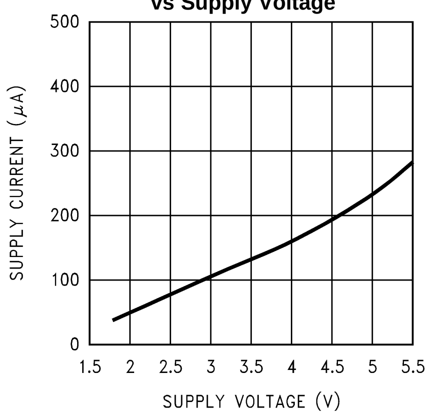


Figure 4.

Supply Current vs Temperature

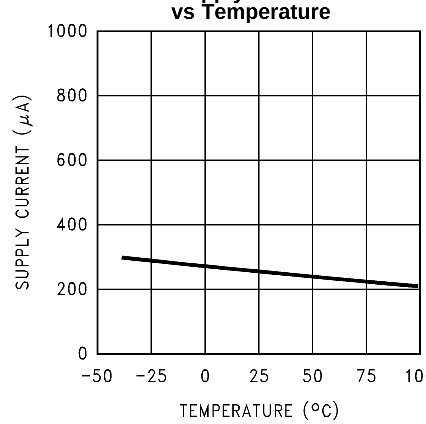


Figure 5.

Output Source Resistance vs Supply Voltage

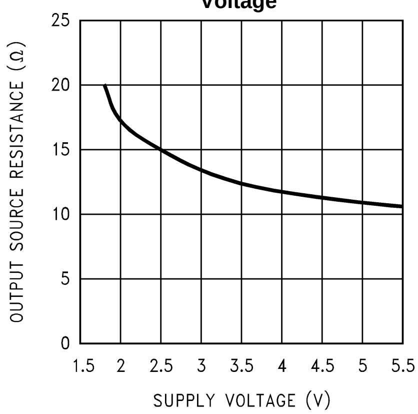


Figure 6.

Output Source Resistance vs Temperature

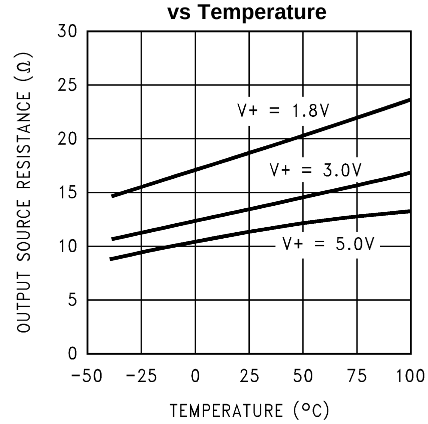


Figure 7.

Typical Performance Characteristics (continued)

(Circuit of Figure 3 V+ = 5V unless otherwise specified)

Output Voltage Drop vs Load Current

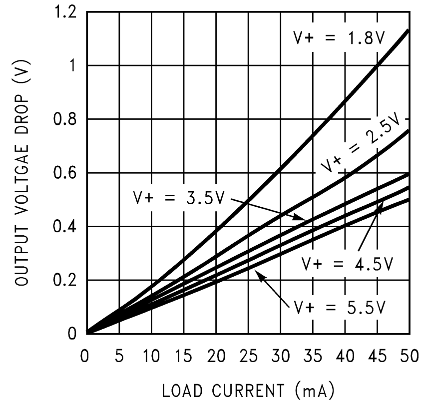


Figure 8.

Efficiency vs Load Current

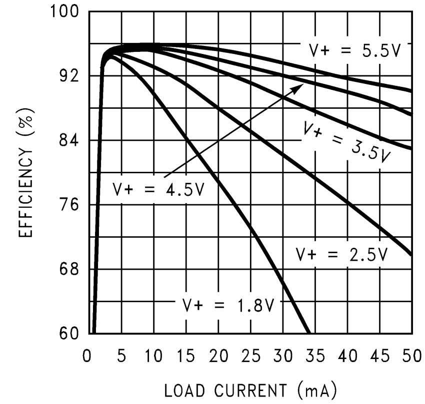


Figure 9.

Oscillator Frequency vs Supply Voltage

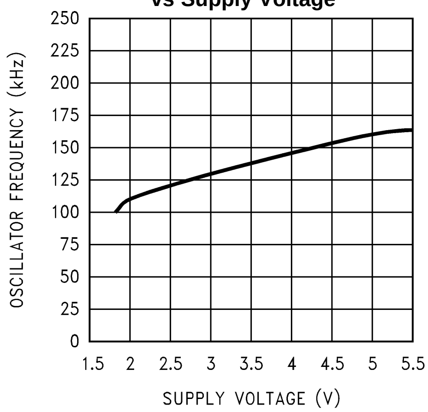


Figure 10.

Oscillator Frequency vs Temperature

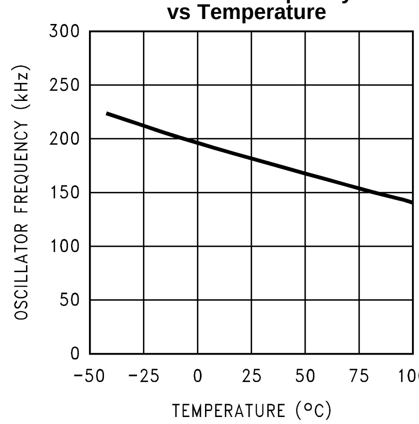


Figure 11.

Shutdown Supply Current vs Temperature

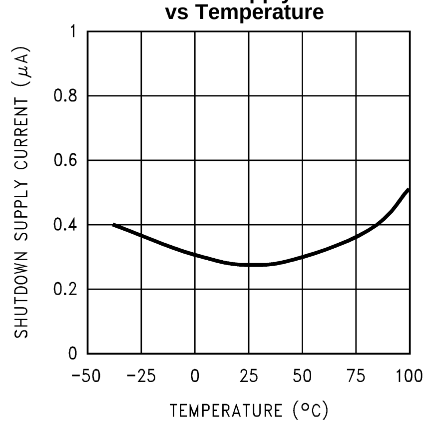


Figure 12.

CONNECTION DIAGRAMS

6-Pin Small Outline Package

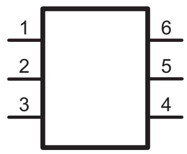


Figure 13. DBV Package Top View

Figure 14. Actual Size

Pin Descriptions

Pin	Name	Function
1	GND	Power supply ground input.
2	OUT	Negative voltage output.
3	CAP−	Connect this pin to the negative terminal of the charge-pump capacitor.
4	SD	Shutdown control pin, tie this pin to V+ in normal operation, and to GND for shutdown.
5	V+	Power supply positive voltage input.
6	CAP+	Connect this pin to the positive terminal of the charge-pump capacitor.

Circuit Description

The LM2664 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 15 illustrates the voltage conversion scheme. When S_1 and S_3 are closed, C_1 charges to the supply voltage V+. During this time interval, switches S_2 and S_4 are open. In the second time interval, S_1 and S_3 are open; at the same time, S_2 and S_4 are closed, C_1 is charging C_2. After a number of cycles, the voltage across C_2 will be pumped to V+. Since the anode of C_2 is connected to ground, the output at the cathode of C_2 equals −(V+) when there is no load current. The output voltage drop when a load is added is determined by the parasitic resistance ($R_{ds(on)}$ of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors. Details will be discussed in the following application information section.

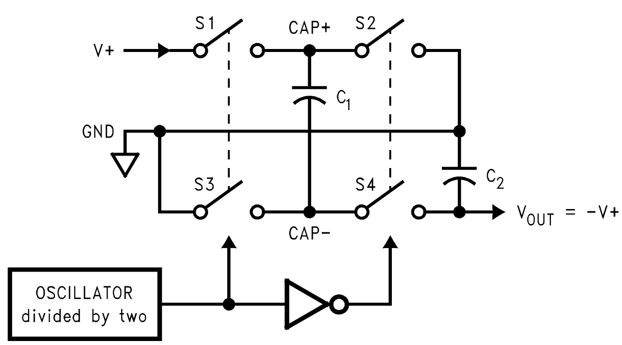


Figure 15. Voltage Inverting Principle

Application Information

SIMPLE NEGATIVE VOLTAGE CONVERTER

The main application of LM2664 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in the Basic Application Circuits. The range of the input supply voltage is 1.8V to 5.5V.

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals −(V+). The output resistance R_{out} is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance and ESR of C_1 and C_2. Since the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 will be multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation of R_{out} is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2}$$

where R_{SW} is the sum of the ON resistance of the internal MOSFET switches shown in Figure 15.

High capacitance, low ESR capacitors will reduce the output resistance.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the output capacitor C_2:

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2}$$

Again, using a low ESR capacitor will result in lower ripple.

SHUTDOWN MODE

A shutdown ($\overline{SD}$) pin is available to disable the device and reduce the quiescent current to 1µA. Applying a voltage less than 20% of V+ to the $\overline{SD}$ pin will bring the device into shutdown mode. While in normal operating mode, the pin is connected to V+.

CAPACITOR SELECTION

As discussed in the *Simple Negative Voltage Converter* section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_L{}^2 R_L}{I_L{}^2 R_L + I_L{}^2 R_{OUT} + I_Q (V+)}$$

Where I_Q(V+) is the quiescent power loss of the IC device, and $I_L{}^2R_{out}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

The selection of capacitors is based on the specifications of the dropout voltage (which equals I_{out} R_{out}), the output voltage ripple, and the converter efficiency. Low ESR capacitors are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

Table 1. Low ESR Capacitor Manufacturers

Manufacturer	Phone	Capacitor Type
Nichicon Corp.	(708)-843-7500	PL & PF series, through-hole aluminum electrolytic
AVX Corp.	(803)-448-9411	TPS series, surface-mount tantalum
Sprague	(207)-324-4140	593D, 594D, 595D series, surface-mount tantalum
Sanyo	(619)-661-6835	OS-CON series, through-hole aluminum electrolytic
Murata	(800)-831-9172	Ceramic chip capacitors
Taiyo Yuden	(800)-348-2496	Ceramic chip capacitors
Tokin	(408)-432-8020	Ceramic chip capacitors

Other Applications

PARALLELING DEVICES

Any number of LM2664s can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor C_1, while only one output capacitor C_{out} is needed as shown in Figure 16. The composite output resistance is:

$$R_{OUT} = \frac{R_{OUT} \text{ of each LM2664}}{\text{Number of Devices}}$$

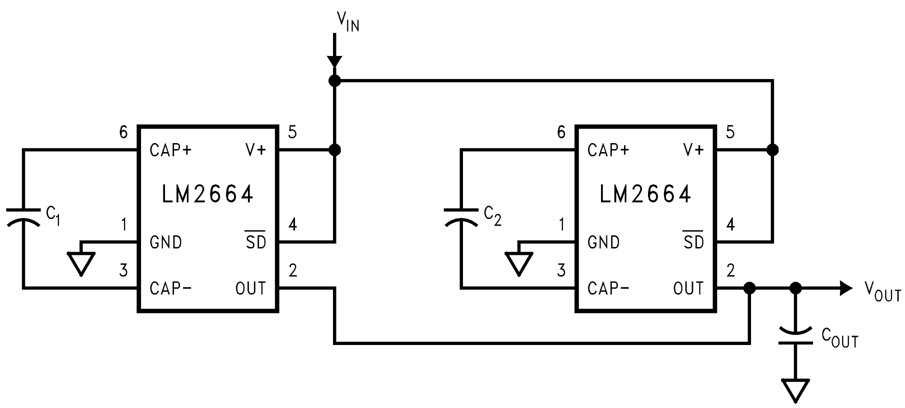


Figure 16. Lowering Output Resistance by Paralleling Devices

CASCADING DEVICES

Cascading the LM2664s is an easy way to produce a greater negative voltage (e.g. A two-stage cascade circuit is shown in Figure 17).

If n is the integer representing the number of devices cascaded, the unloaded output voltage V_{out} is ($-nV_{in}$). The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = nR_{out\_1} + n/2\ R_{out\_2} + ... + R_{out\_n} \qquad (1)$$

Note that, the number of n is practically limited since the increasing of n significantly reduces the efficiency, and increases the output resistance and output voltage ripple.

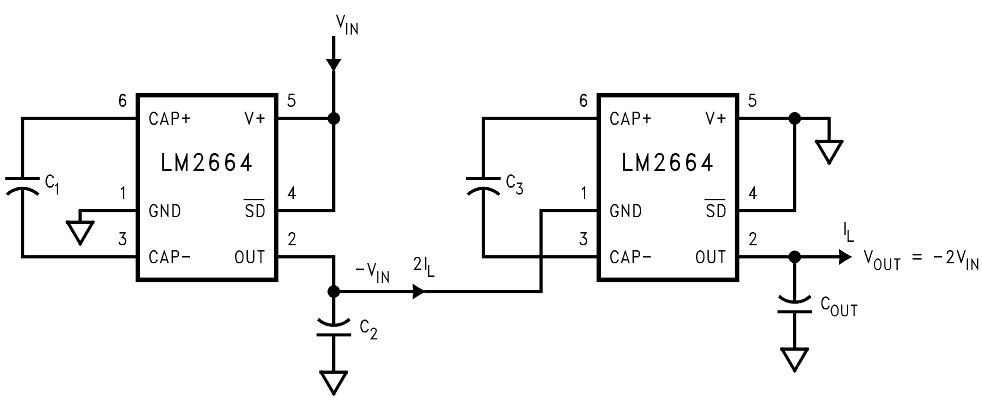


Figure 17. Increasing Output Voltage by Cascading Devices

COMBINED DOUBLER AND INVERTER

In Figure 18, the LM2664 is used to provide a positive voltage doubler and a negative voltage converter. Note that the total current drawn from the two outputs should not exceed 50 mA.

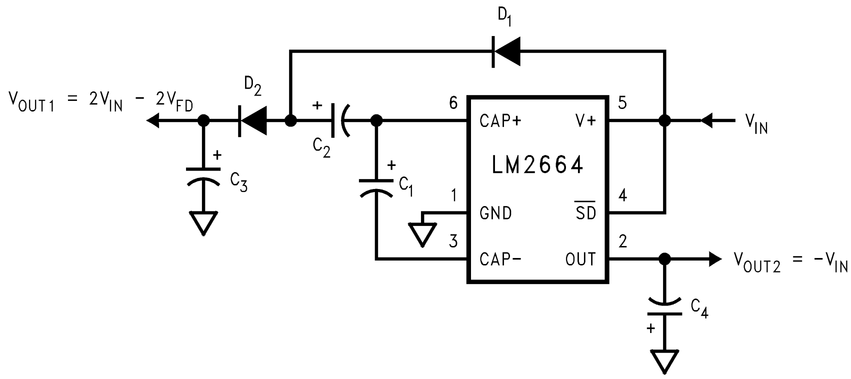


Figure 18. Combined Voltage Doubler and Inverter

REGULATING V_{OUT}

It is possible to regulate the negative output of the LM2664 by use of a low dropout regulator (such as LP2980). The whole converter is depicted in Figure 19. This converter can give a regulated output from −1.8V to −5.5V by choosing the proper resistor ratio:

$$V_{out} = V_{ref} (1 + R_1/R_2) \quad (2)$$

where, $V_{ref} = 1.23V$ (3)

Note that, the following conditions must be satisfied simultaneously for worst case design:

$V_{in\_min} > V_{out\_min} + V_{drop\_max}$ (LP2980) (4)

$+ I_{out\_max} \times R_{out\_max}$ (LM2664) (5)

$V_{in\_max} < V_{out\_max} + V_{drop\_min}$ (LP2980) (6)

$+ I_{out\_min} \times R_{out\_min}$ (LM2664) (7)

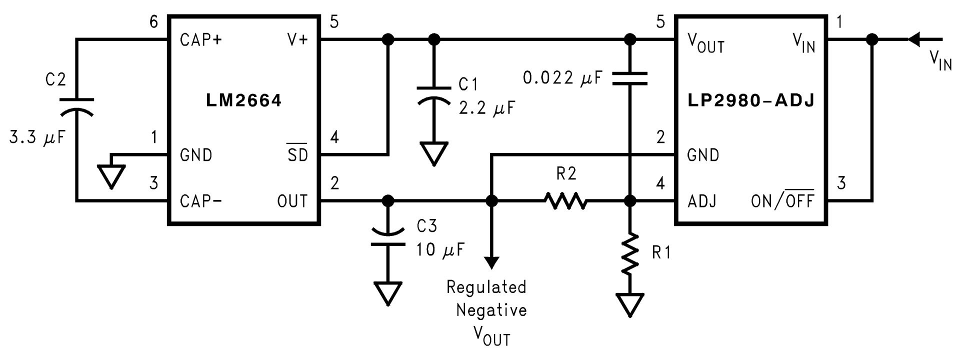


Figure 19. Combining LM2664 with LP2980 to Make a Negative Adjustable Regulator

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2664M6	ACTIVE	SOT-23	DBV	6	1000	TBD	Call TI	Call TI	-40 to 85	S03A	Samples
LM2664M6/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S03A	Samples
LM2664M6X	ACTIVE	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 85	S03A	Samples
LM2664M6X/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S03A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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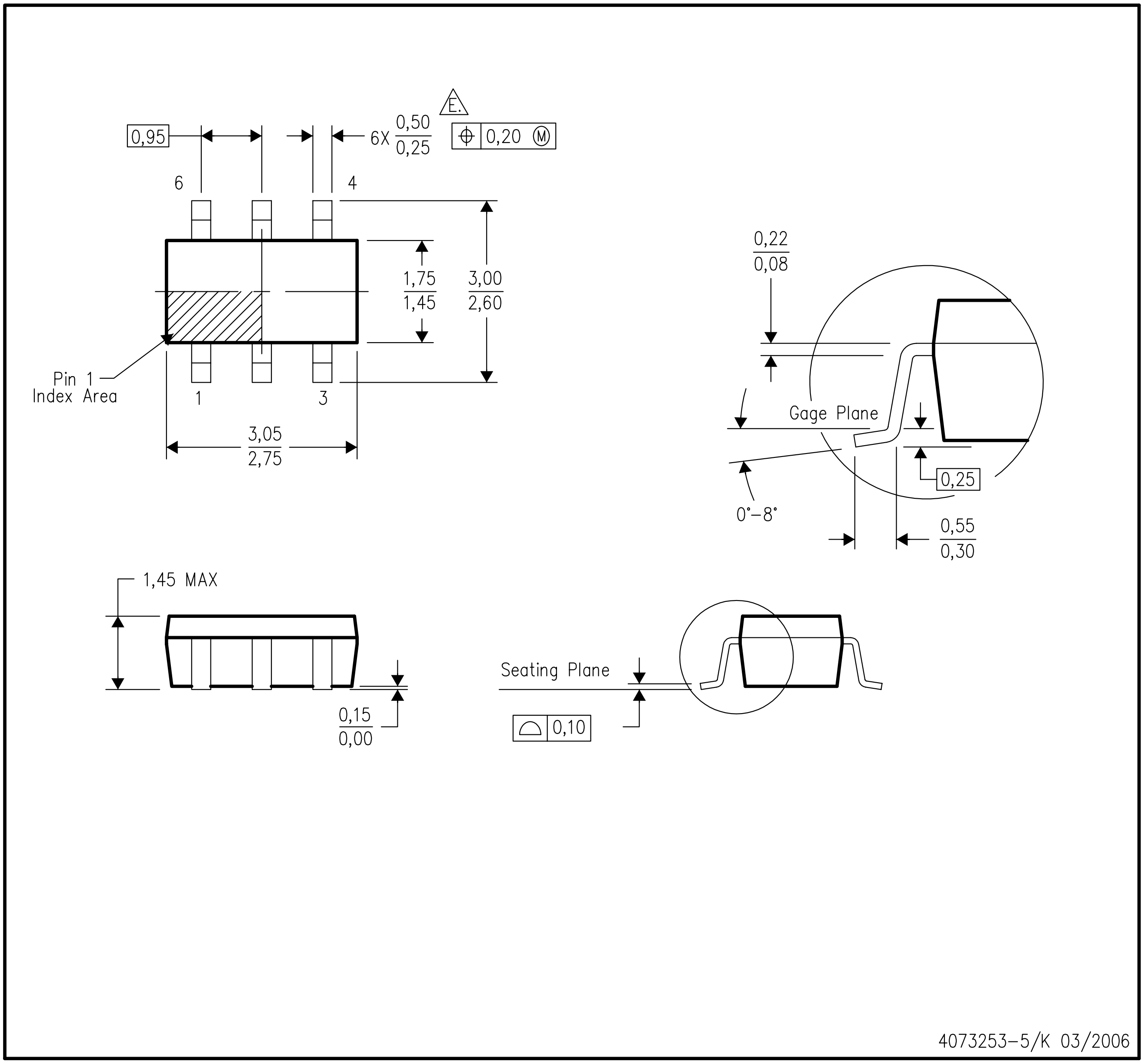
DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

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